Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the present application.

Listing of the Claims:

1. (Currently Amended) A method of fabricating a MOSFET with pocket regions, comprising:

forming a gate electrode layer on a semiconductor substrate;

forming lightly doped drain regions in the semiconductor substrate adjacent the gate electrode layer;

forming a device isolation region on the semiconductor substrate surrounding the lightly doped drain regions adjacent the gate electrode layer;

forming a blocking pattern on the semiconductor substrate, the blocking pattern being adjacent and spaced apart from the gate electrode layer a predetermined distance and exposing portions of the semiconductor substrate adjacent sidewalls of the gate electrode layer and extending over the device isolation region and onto the lightly doped drain regions adjacent the gate electrode layer; and

forming pocket regions in the semiconductor substrate by implanting impurity ions at an oblique tilt angle into a surface of the semiconductor substrate between the blocking pattern and the gate electrode layer using the gate electrode layer and the blocking pattern as an ion implantation mask to define a width of the pocket regions.

2. (Original) The method of Claim 1, further comprising;

removing the blocking pattern;

forming spacers on the sidewalls of the gate electrode layer; and

implanting impurity ions using the gate electrode layer having the spacers as an ion implantation mask to form deep source/drain regions in the semiconductor substrate.

3. (Original) The method of Claim 1, wherein the semiconductor substrate is a single crystalline silicon substrate and/or a silicon-on-insulator substrate.

4. (Original) The method of Claim 1, wherein the gate electrode layer comprises polysilicon, a silicon compound and/or a metal.

5. (Currently Amended) ~~The method of Claim 1,~~ A method of fabricating a MOSFET with pocket regions, comprising:

forming a gate electrode layer on a semiconductor substrate;

forming lightly doped drain regions in the semiconductor substrate adjacent the gate electrode layer;

forming a blocking pattern on the semiconductor substrate, the blocking pattern being adjacent and spaced apart from the gate electrode layer a predetermined distance and exposing portions of the semiconductor substrate adjacent sidewalls of the gate electrode layer; and

forming pocket regions in the semiconductor substrate by implanting impurity ions using the gate electrode layer and the blocking pattern as an ion implantation mask;

wherein forming the blocking pattern comprises:

forming a first blocking layer on a surface of the semiconductor substrate where the gate electrode layer is formed;

depositing a second blocking layer on the first blocking layer, the second blocking layer having an etch selectivity with respect to the first blocking layer;

forming a photoresist pattern to be spaced apart from the sidewalls of the gate electrode layer by a predetermined distance, so as to expose portions of the second blocking layer between the photoresist pattern and the sidewalls of the gate electrode layer and a portion of the second blocking layer over the gate electrode layer;

etching the exposed second blocking layer and the first blocking layer using the photoresist pattern as an etch mask; and

removing the photoresist pattern.

6. (Original) The method of Claim 5, wherein depositing the first blocking layer is preceded by forming a first insulating layer, which has an etch selectivity with respect to the first blocking layer, on the surface of the semiconductor substrate including the exposed surface of the gate electrode layer.

7. (Original) The method of Claim 6, wherein the first insulating layer is a silicon oxide layer, the first blocking layer is a silicon nitride layer, and the second blocking layer is a silicon oxide layer.

8. (Original) The method of Claim 6, wherein the first insulating layer is a silicon oxide layer, the first blocking layer is SiON layer and/or a SiBN layer, and the second blocking layer is a silicon oxide layer.

9. (Original) The method of Claim 5, wherein etching the second blocking layer and the first blocking layer further comprises removing the first blocking layer that remains on the sidewalls of the gate electrode layer.

10. (Original) The method of Claim 1, wherein, when the pocket regions are formed, the area of the pocket regions is controlled by adjusting a thickness of the blocking pattern and the distance between the sidewalls of the gate electrode layer and the blocking pattern.

11. (Currently Amended) The method of Claim 2, wherein implanting impurity ions using the gate electrode layer having the spacers as an ion implantation mask to form deep source/drain regions in the semiconductor substrate is followed by forming a metal silicide layer on a surface of the gate electrode layer and the source/drain regions.

12. (Original) The method of Claim 1, wherein forming a blocking pattern on the semiconductor substrate comprises forming a blocking pattern comprising a plurality of blocking layers.

13. (Original) The method of Claim 1, wherein the blocking pattern has a thickness b, the pocket regions are to be formed to have a width d', the impurity ions are implanted at a tilt angle θ and an expected range of Rp, the predetermined distance c that the blocking pattern is spaced apart from the sidewalls comprises $c = d' + b/\tan(90-\theta) + Rp\sin\theta$.

14. (Original) The method of Claim 1, wherein forming lightly doped drains is followed by forming pocket regions.

15. (Original) The method of Claim 1, wherein forming pocket regions is followed by forming lightly doped drains.